

## TITLE OF THE INVENTION

### METHOD FOR FABRICATING A CHIP SCALE PACKAGE USING WAFER LEVEL PROCESSING AND DEVICES RESULTING THEREFROM

## CROSS-REFERENCE TO RELATED APPLICATIONS

11/10/04  
[0001] This application is a divisional of application Serial No. 09/917,127 filed July 27, 2001, <sup>now US Patent No. 6,780,746 published August 24, 2004</sup> pending, which is a divisional of application Serial No. 09/586,243, filed June 2, 2000, <sup>now US Patent No. 6,717,245 published June 2, 2000</sup> pending.

## BACKGROUND OF THE INVENTION

[0002] Field of the Invention: The present invention relates to semiconductor devices and methods for fabricating semiconductor devices. More specifically, the invention relates to a method for packaging a semiconductor die having conductive elements that protrude at least to the surface of a covering or encapsulation of the die active surface.

[0003] State of the Art: In semiconductor manufacture, a single semiconductor die or chip including a plurality of integrated circuits on an active surface thereof is typically mounted within a sealed package of a silicon-filled epoxy formed thereabout by a process known as transfer-molding. The package generally protects the die from physical damage and from contaminants, such as moisture or chemicals, found in the surrounding environment. The package also provides a lead system for connecting the electrical devices (integrated circuits) formed on the die to a printed circuit board or other higher-level packaging.

[0004] Packaged semiconductor dice containing integrated circuits for a broad range of purposes are currently mass produced. Even slight savings in the cost of packaging one such semiconductor die circuit can generate significant overall cost savings to the manufacturer, due to large production volumes, if the reduced-cost packaging affords required package integrity. Further, reduction in package size can eliminate size-based restrictions for use of a die on ever more crowded carrier substrates such as printed circuit boards (PCBs), where available "real estate" is at a premium. Therefore, continual cost reductions and quality improvements in the